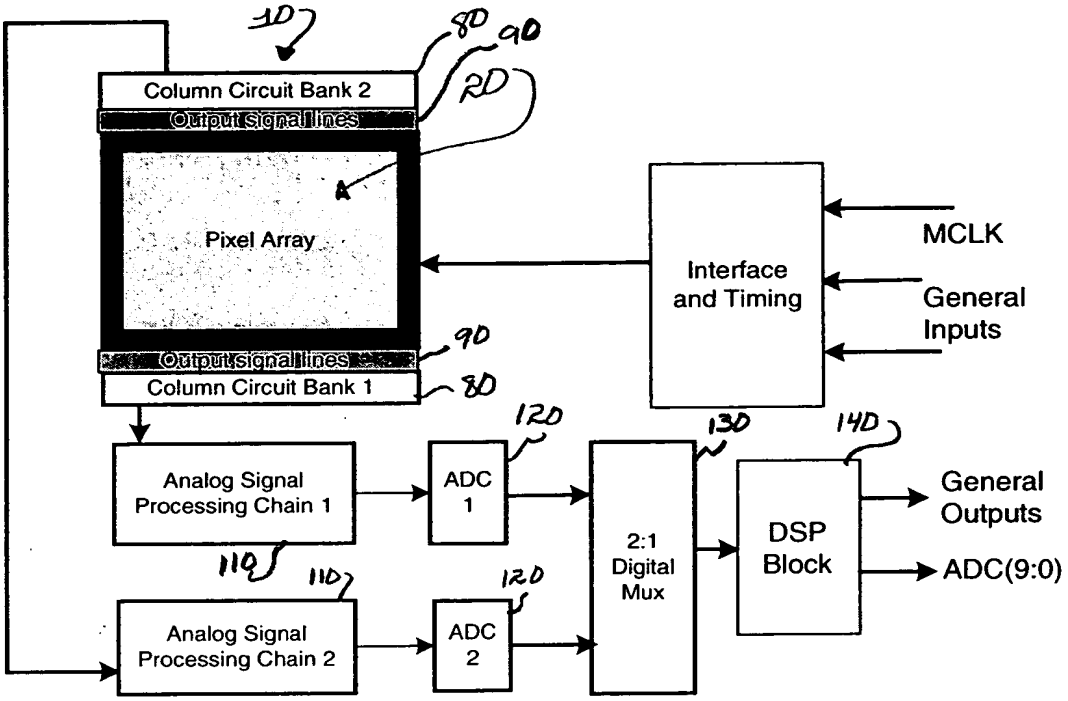


Figure 1 – Sensor Block Diagram

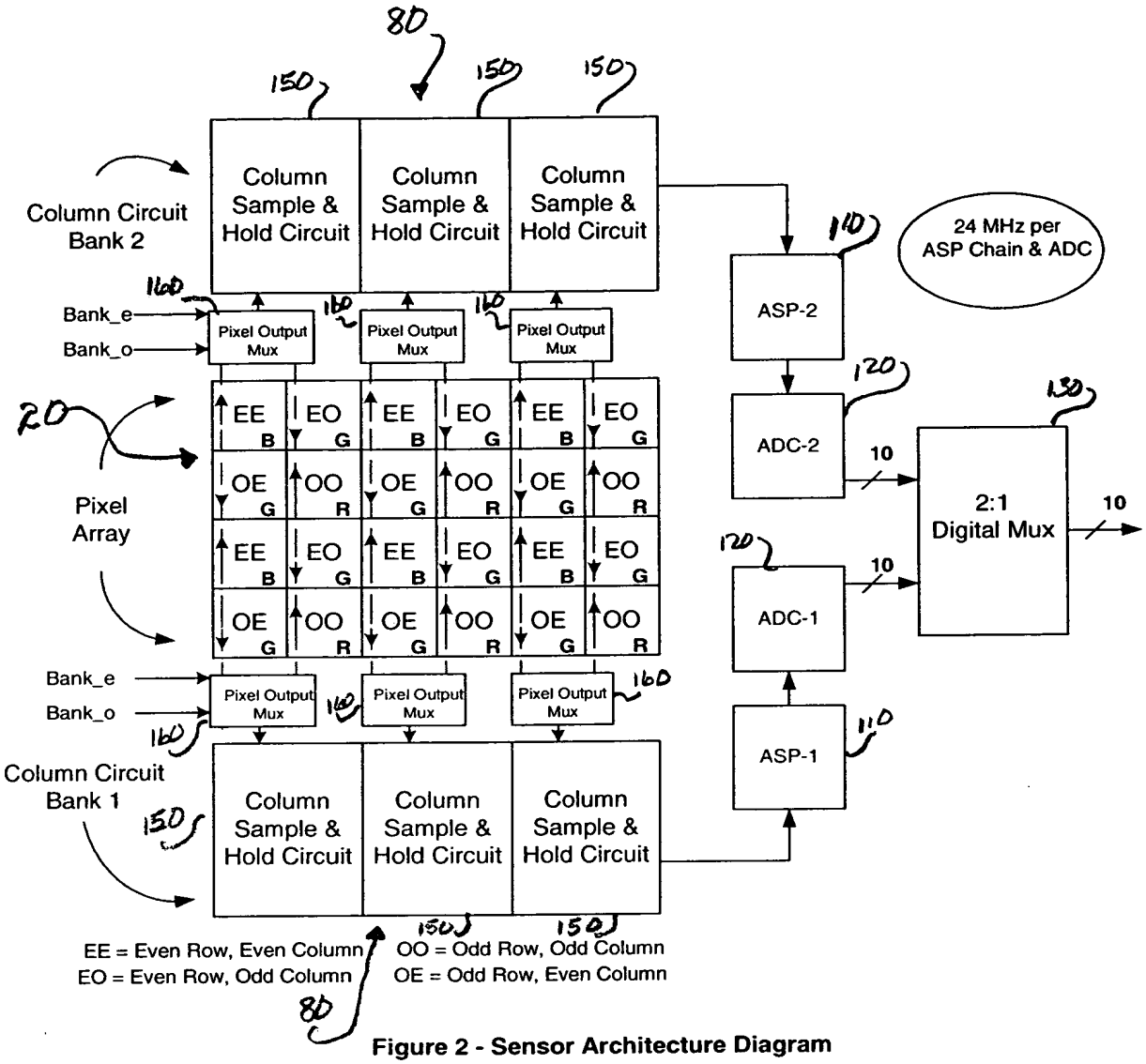
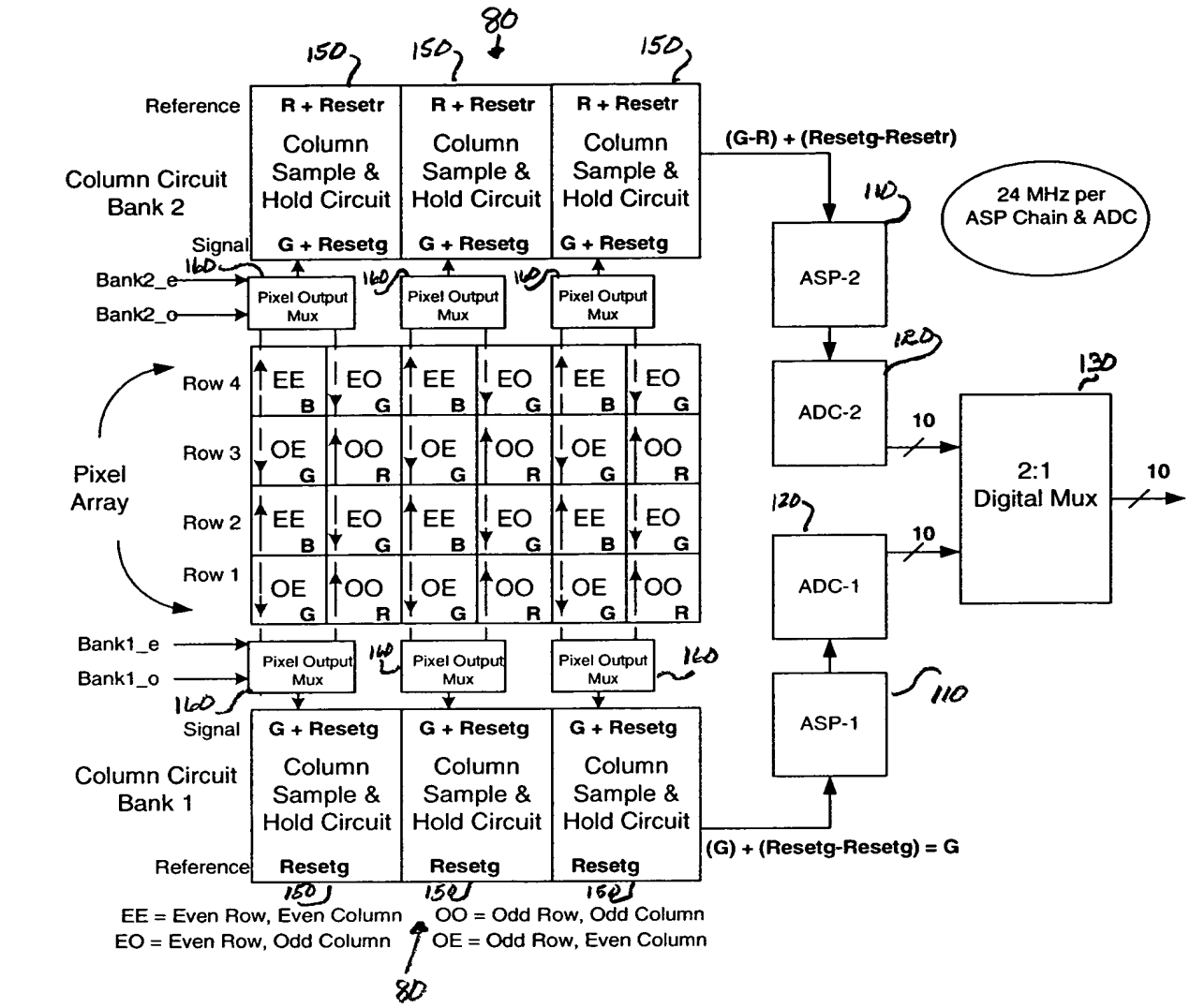


Figure 2 - Sensor Architecture Diagram



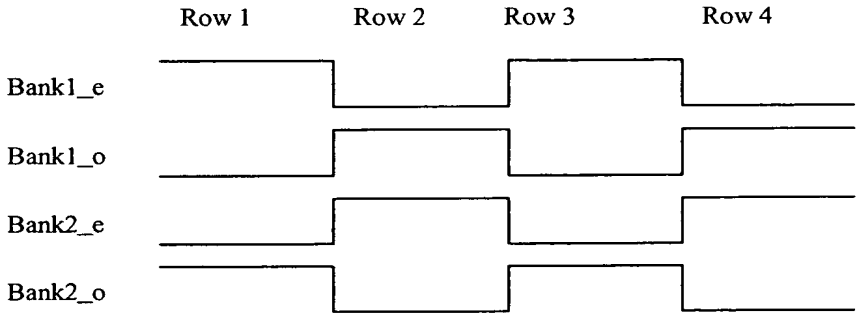


Figure 3 – Sensor Timing for Color Difference Readout

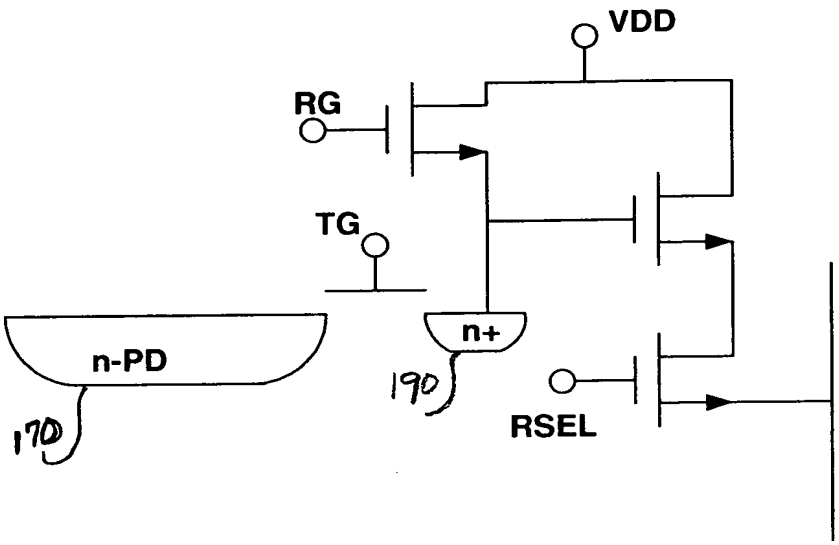


Figure 4 – 4 Transistor Pixel

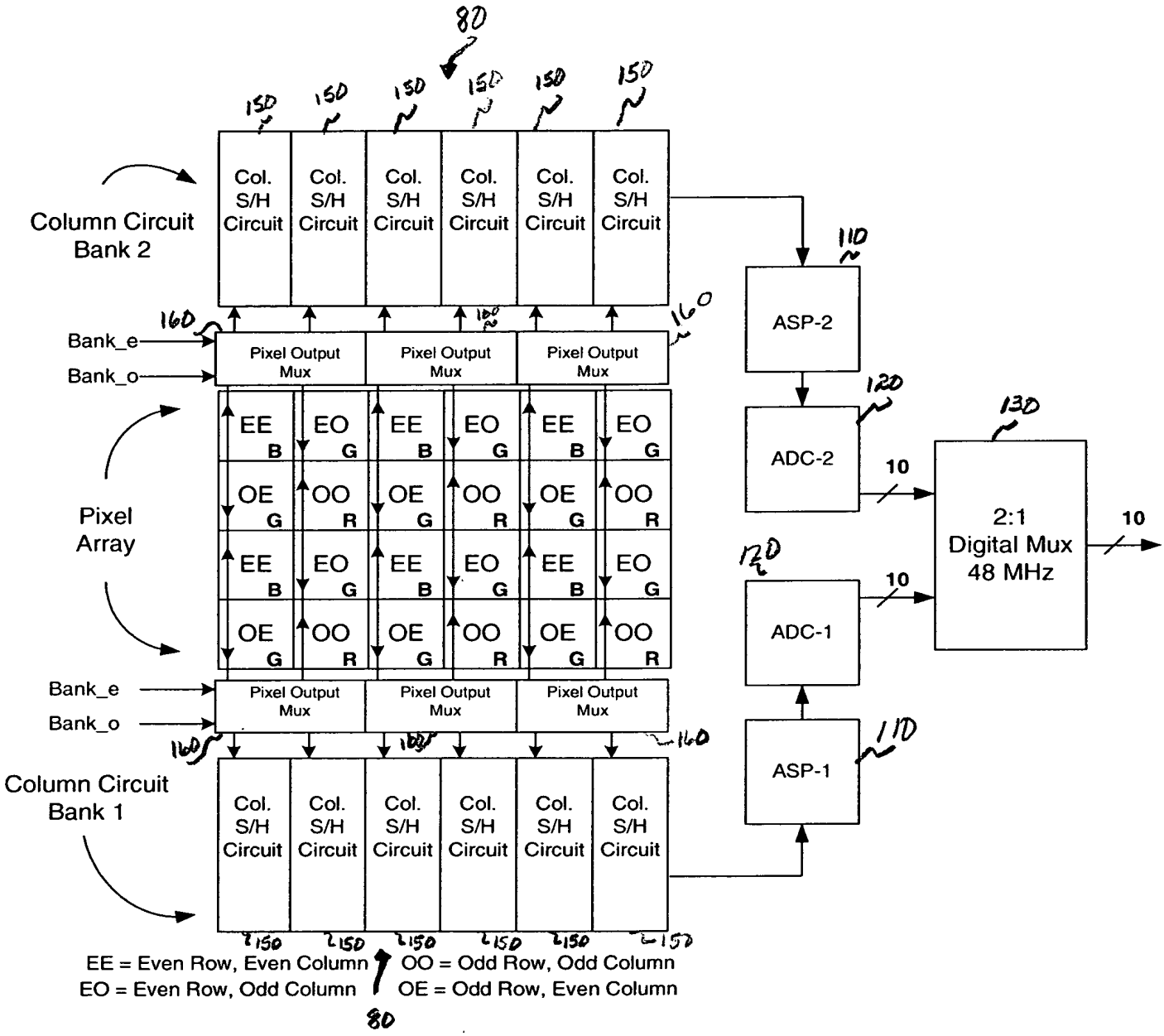


Figure 5a - Sensor Architecture Diagram

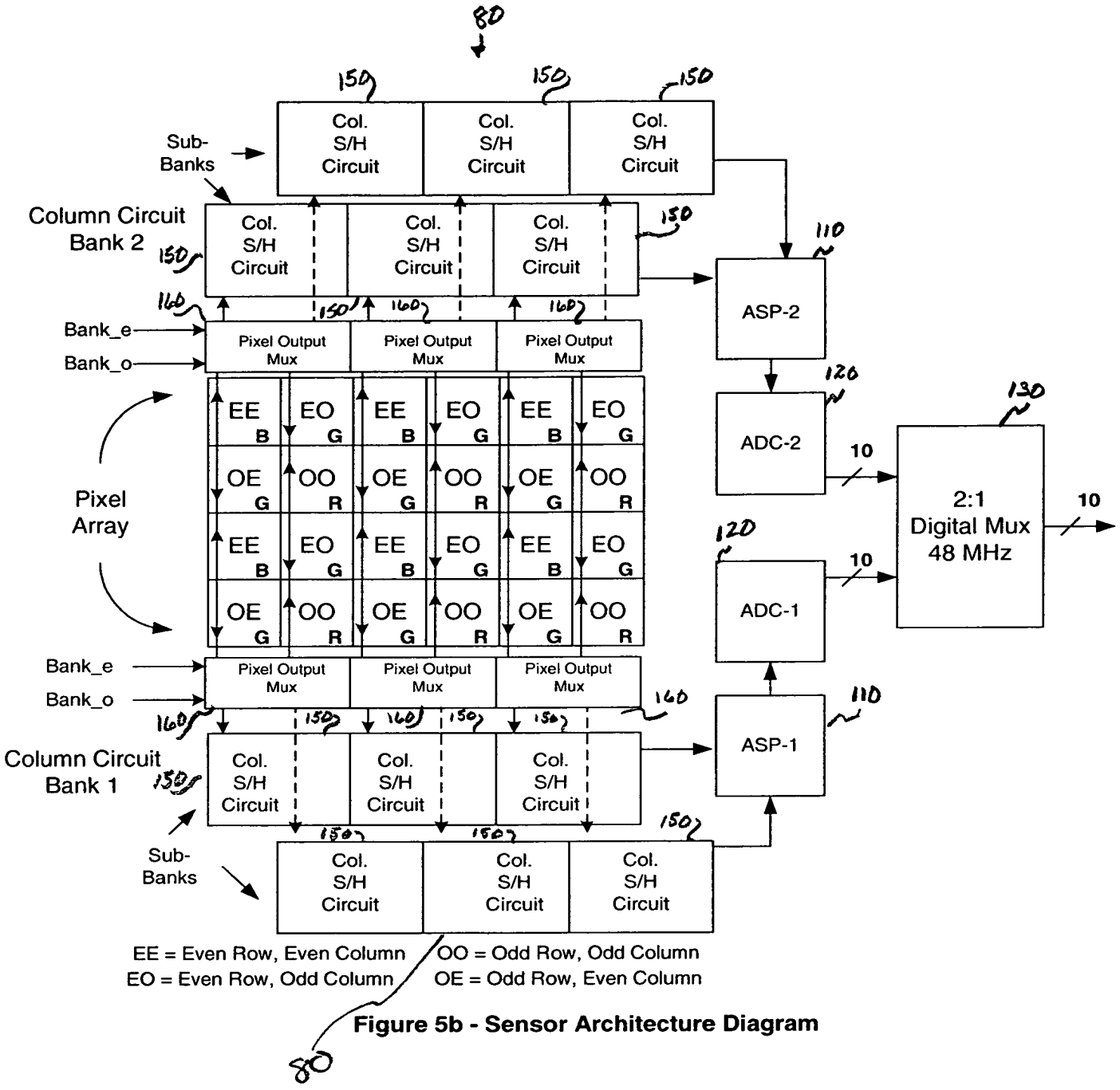
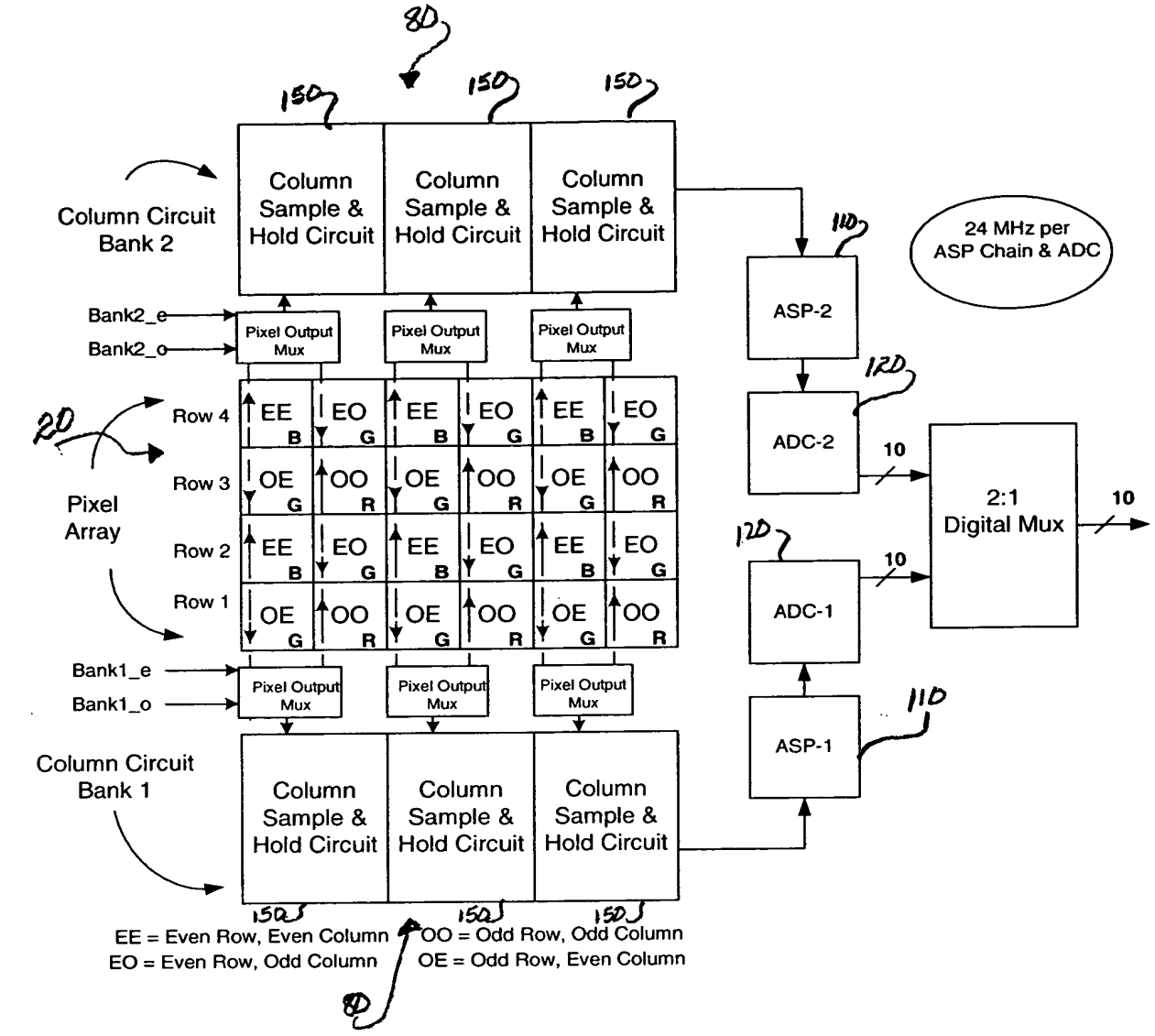


Figure 5b - Sensor Architecture Diagram



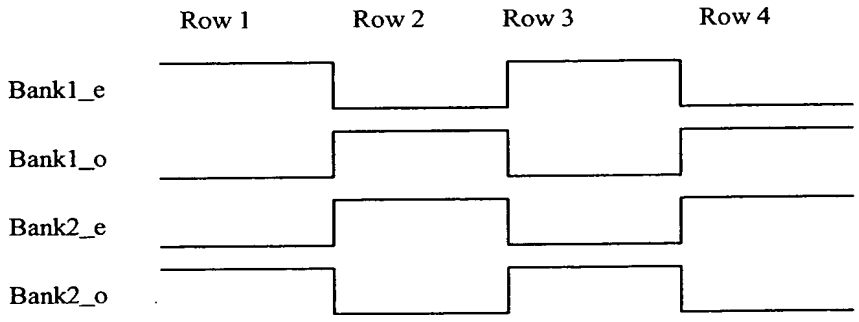
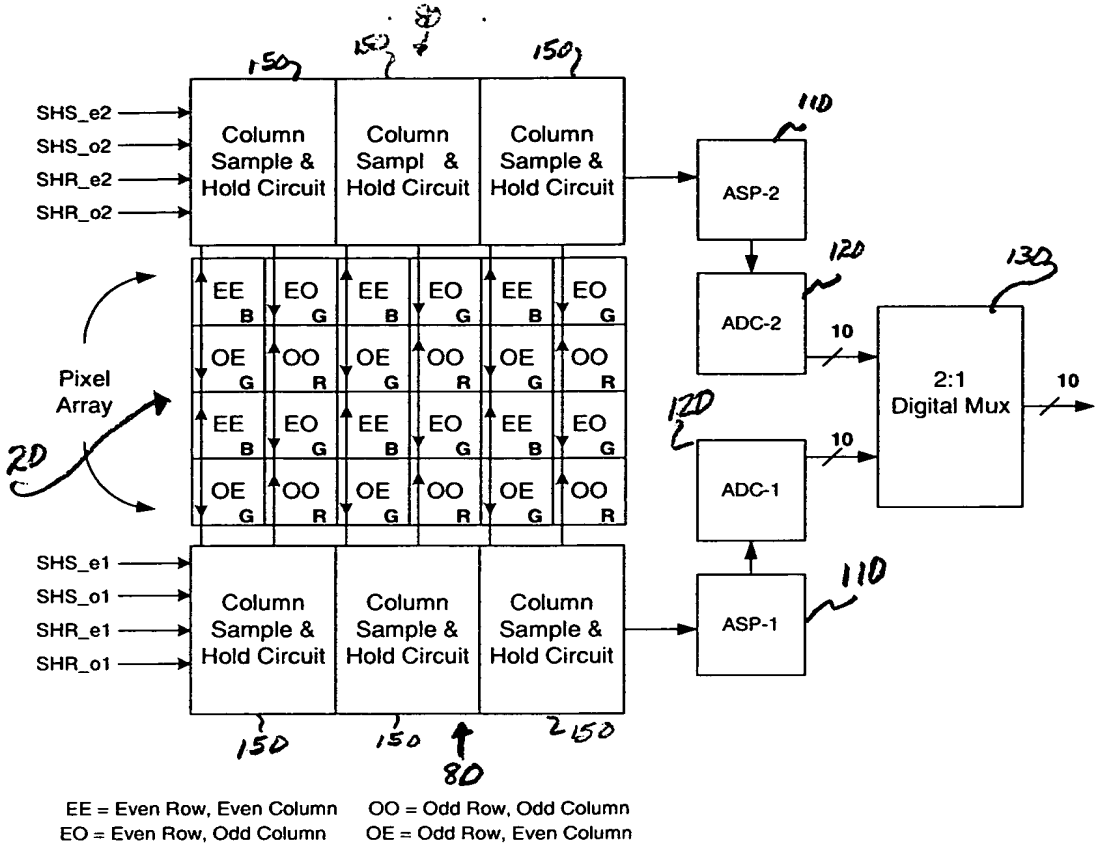


Figure 6a – Pixel Output Multiplexer Timing Diagram for Color Plane Separation



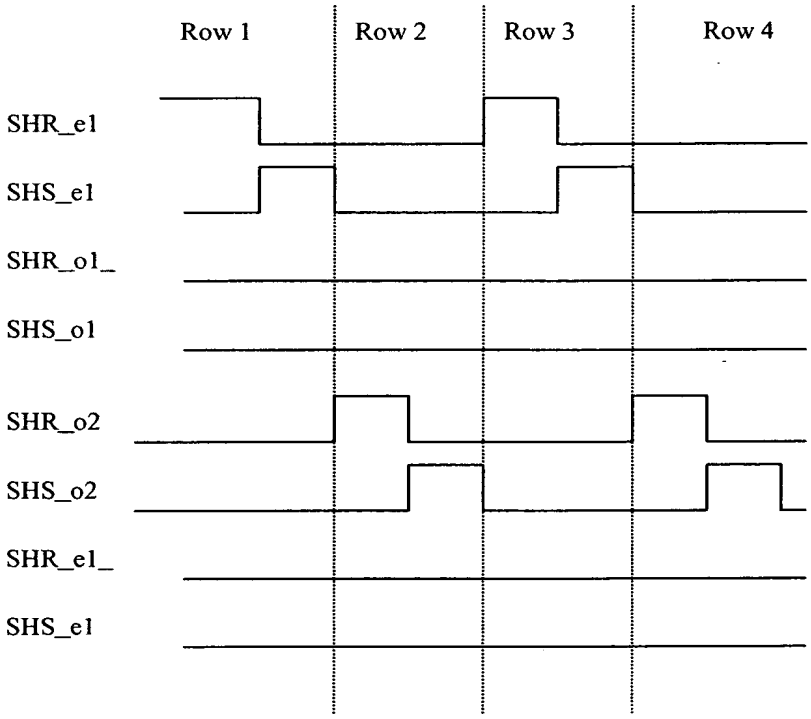


Figure 6b – Pixel Output Multiplexer Timing Diagram for Color Plane Separation

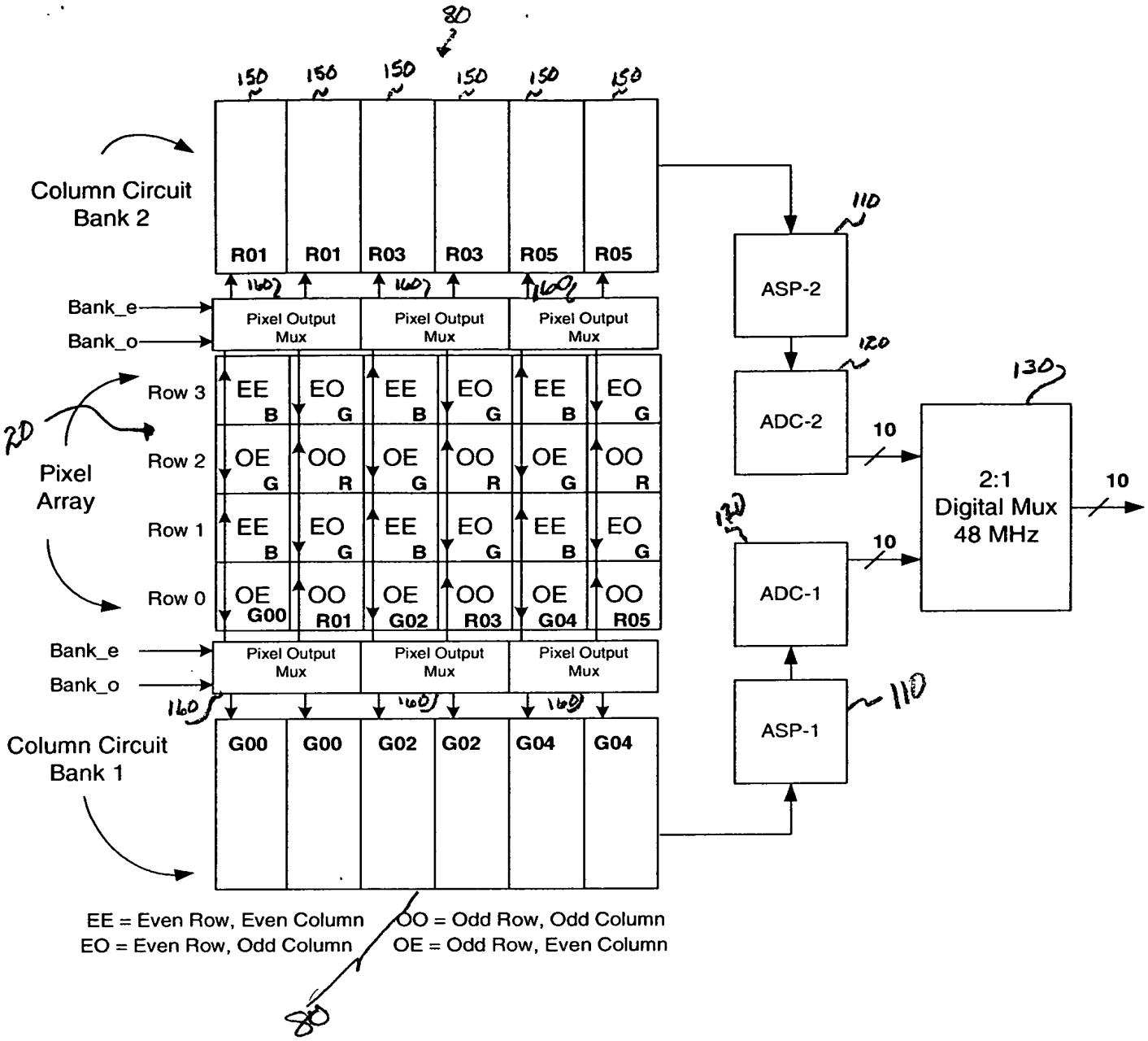


Figure 6c – Sensor Block Diagram for Adjacent Sample Averaging

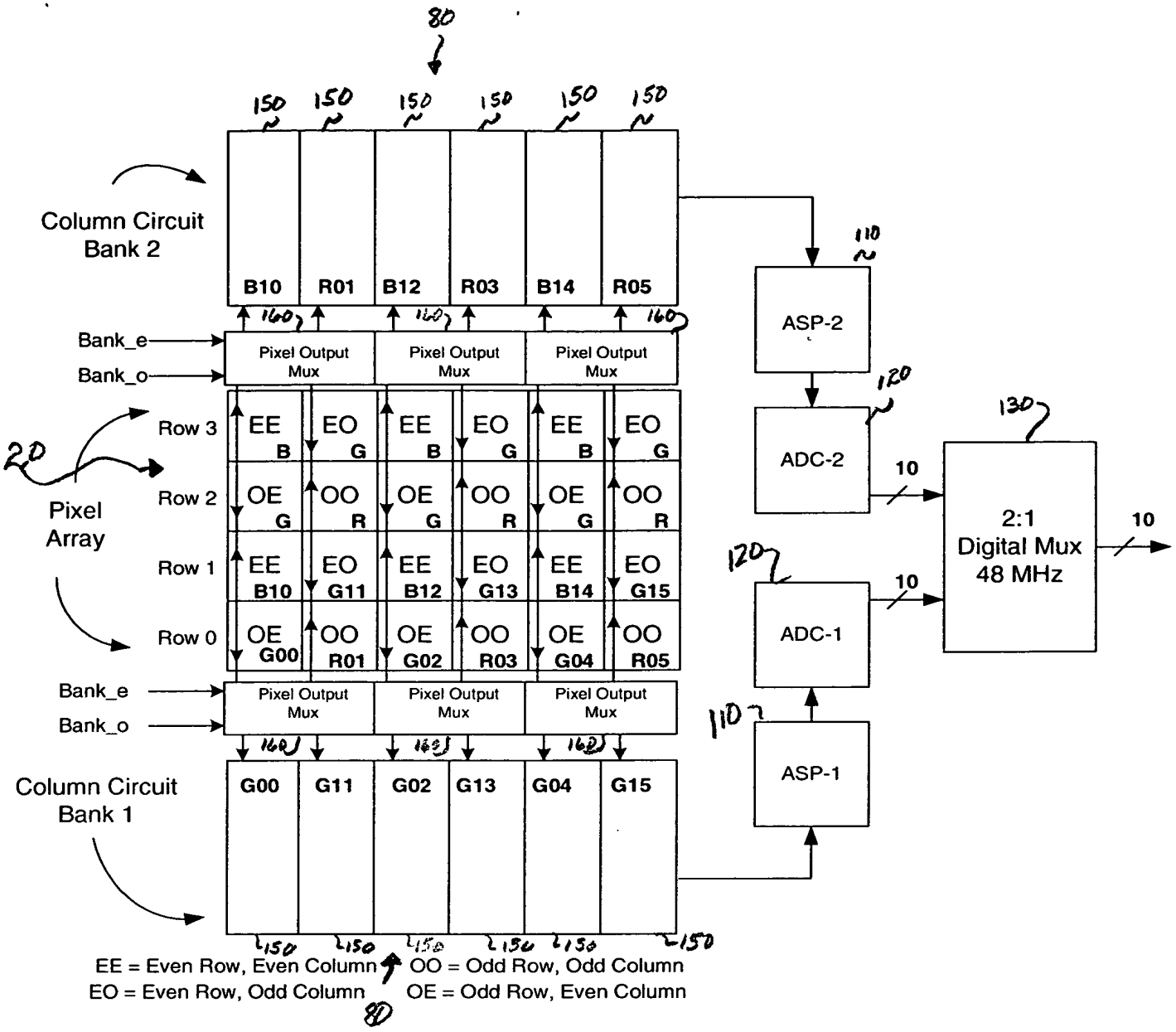


Figure 6d – Sensor Block Diagram for ~~Adjacent Sample Averaging~~ Two Row Readout

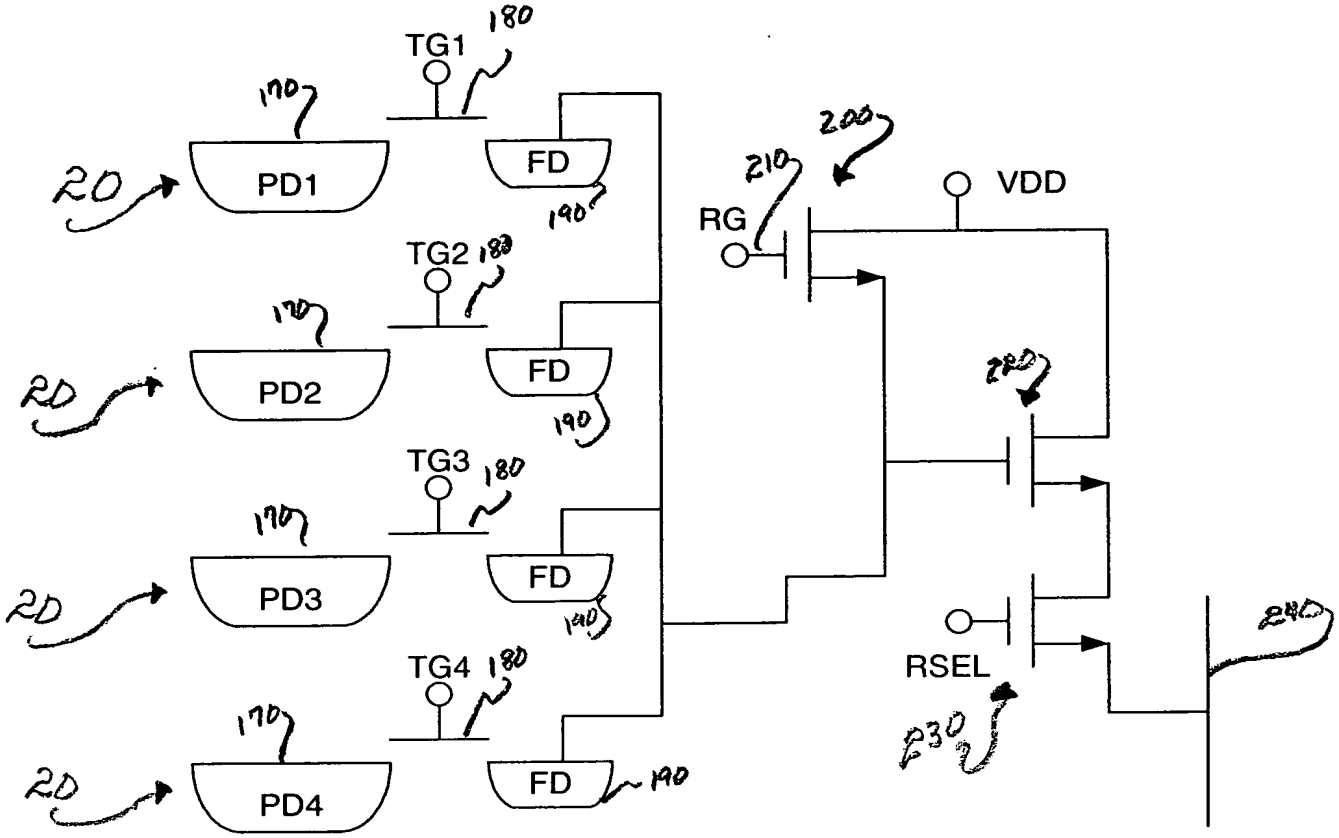


Figure 7: 4-shared Pixel Schematic

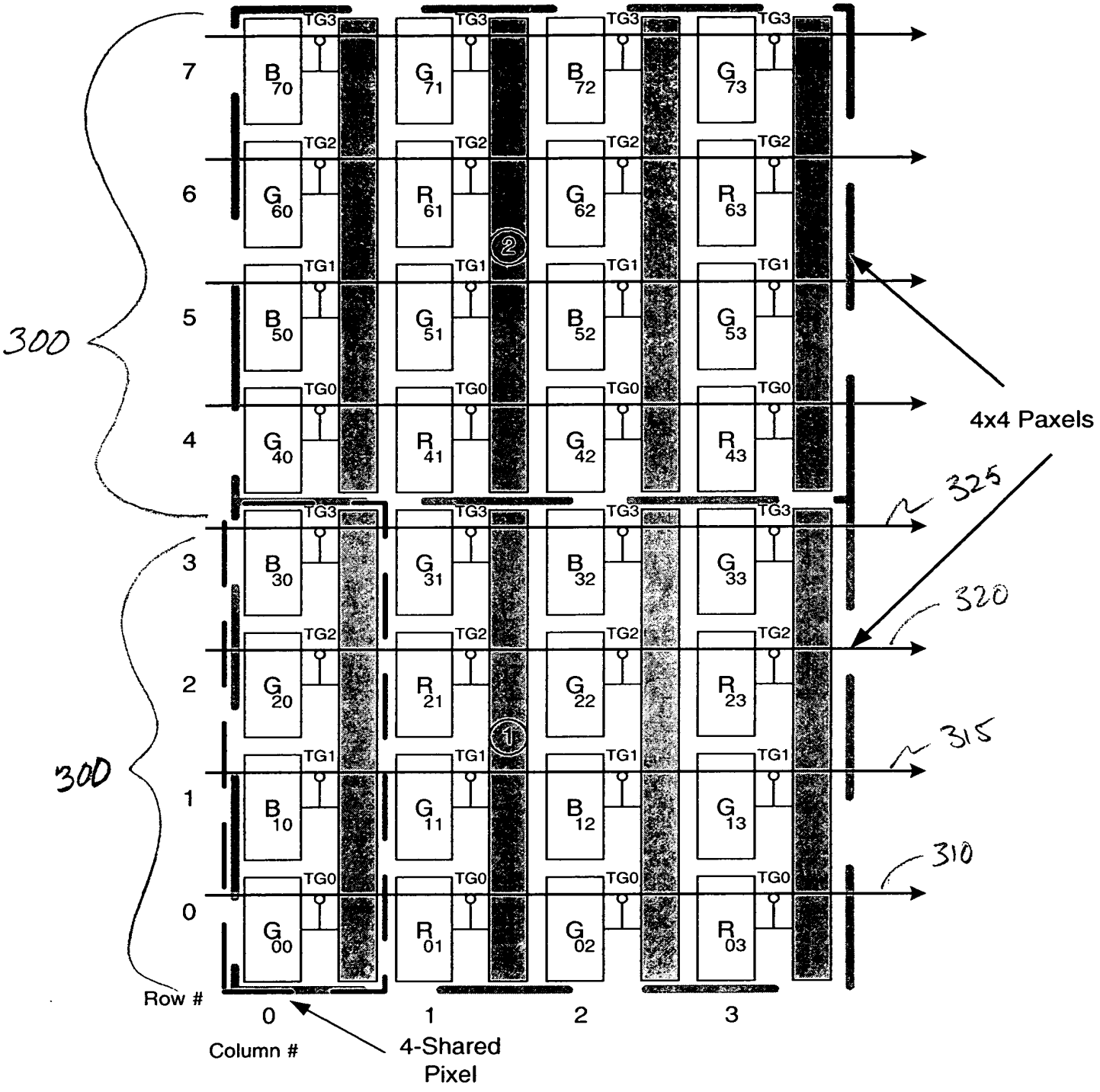


Figure 8a: 4x4 Paxel Diagram

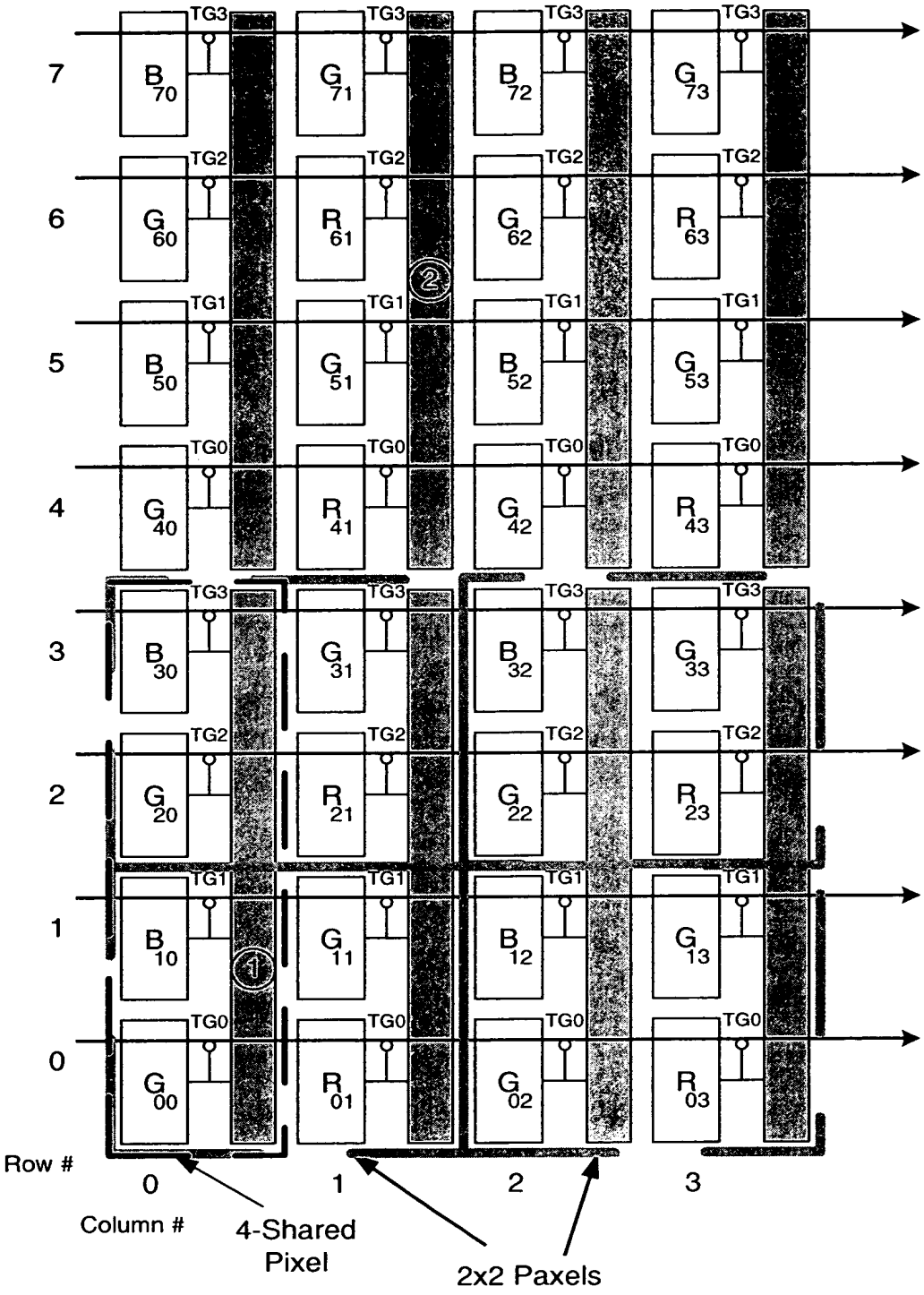


Figure 8b: 2x2 Binning and Decimation

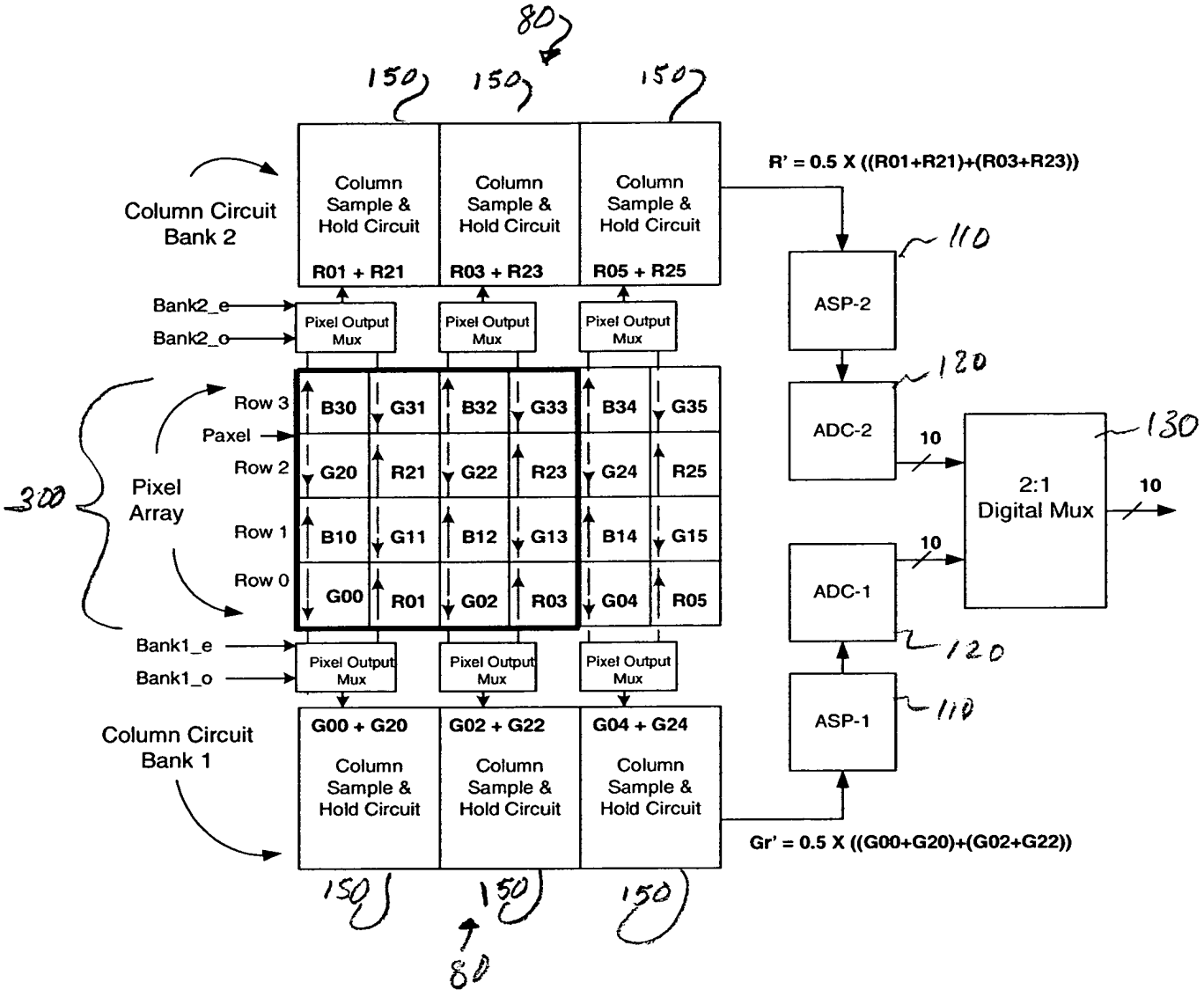

80
150
150
150
Column Circuit Bank 2
Column Sample & Hold Circuit
Column Sample & Hold Circuit
Column Sample & Hold Circuit
R01 + R21
R03 + R23
R05 + R25
R' = 0.5 X ((R01+R21)+(R03+R23))
110
ASP-2
120
ADC-2
10
130
2:1 Digital Mux
10
Bank2_e
Bank2_o
Pixel Output Mux
Pixel Output Mux
Pixel Output Mux
Row 3
Paxel
Row 2
Row 1
Row 0
B30
G31
B32
G33
B34
G35
G20
R21
G22
R23
G24
R25
B10
G11
B12
G13
B14
G15
G00
R01
G02
R03
G04
R05
300
Pixel Array
Bank1_e
Bank1_o
Pixel Output Mux
Pixel Output Mux
Pixel Output Mux
10
ADC-1
120
ASP-1
110
Column Circuit Bank 1
G00 + G20
G02 + G22
G04 + G24
Column Sample & Hold Circuit
Column Sample & Hold Circuit
Column Sample & Hold Circuit
Gr' = 0.5 X ((G00+G20)+(G02+G22))
150
150
150
80

Figure 8c -

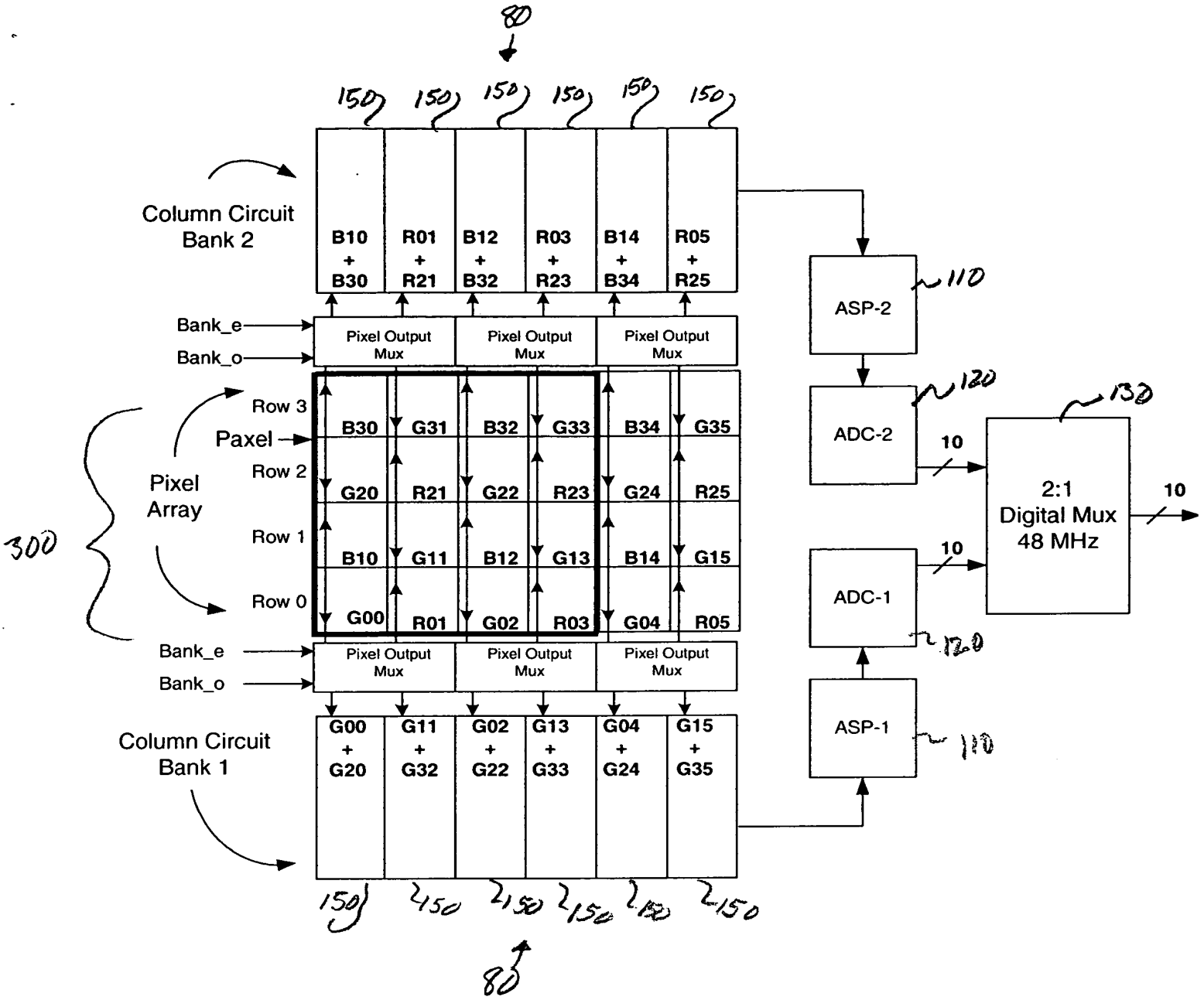


Figure 9 – Sensor Diagram for 16x Resolution Reduction

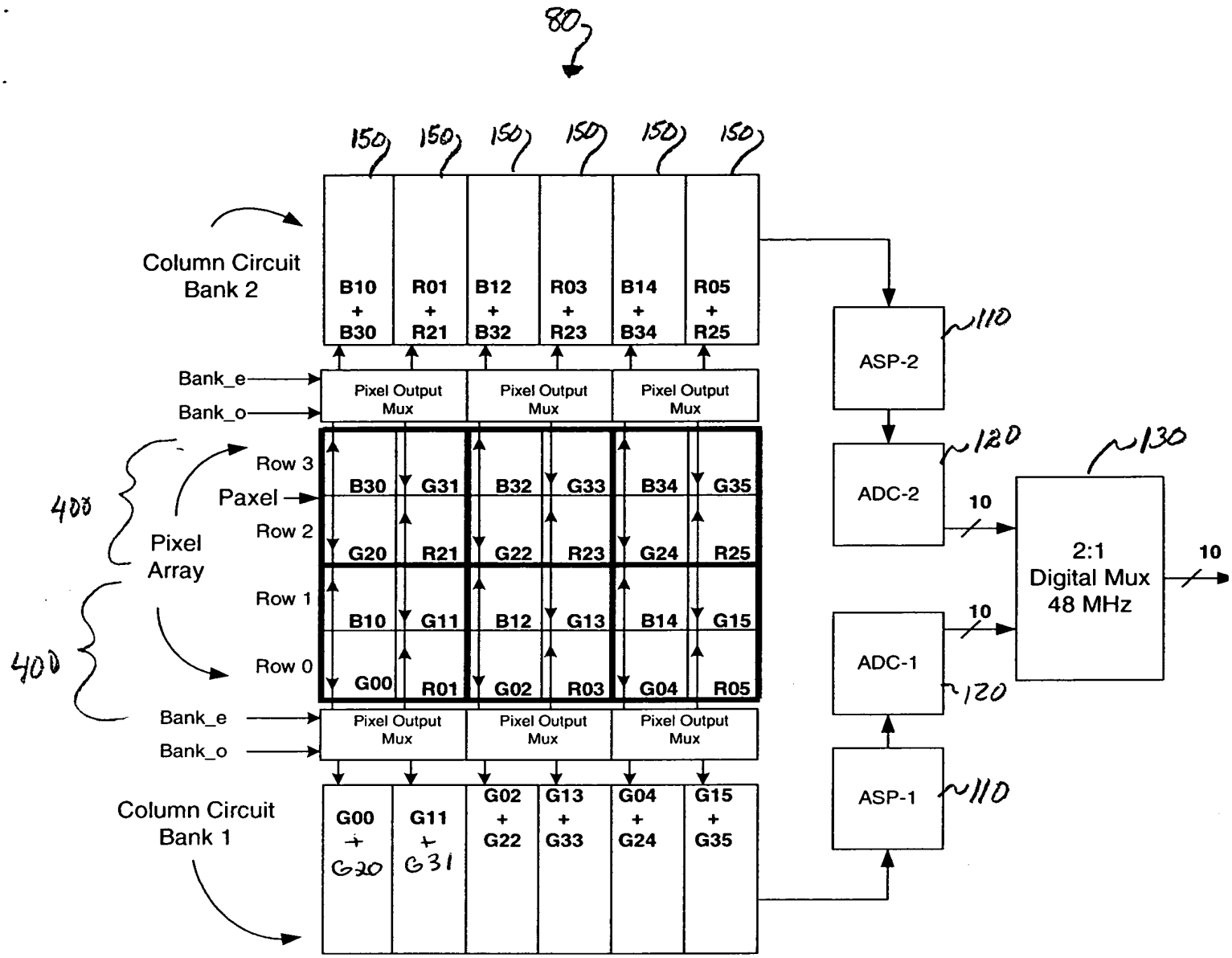


Figure 10 – Sensor Diagram for 4x Resolution Reduction

500

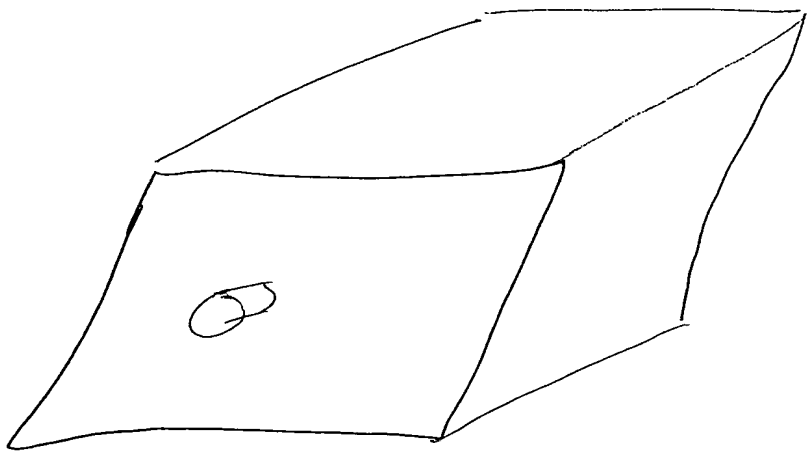


Fig. 11